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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,636	12/19/2001	Yi-Tang Wang	JCLA7952	8257

23900 7590 03/29/2005

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EXAMINER

STOYNOV, STEFAN

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/025,636

Applicant(s)

WANG ET AL.

Examiner

Stefan Stoynov

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5,6,11,12,17 and 18 is/are allowed.
- 6) ☒ Claim(s) 1,2,7,8,13 and 14 is/are rejected.
- 7) ☒ Claim(s) 3,4,9,10,15,16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 7, 8, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cota-Robles in view of Beladi, and further in view of Ichikawa.

Re claim 1, Cota-Robles discloses an operating method, for detecting and solving underflow and overflow (column 1, lines 9-14, column 3, lines 29-31), the method for a transmitter and a receiver to transmit and receive data by using different clock frequencies (column 1, lines 24-26), the receiver receives a plurality of received packages, each of the received packages includes a plurality of data (column 1, lines 19-23), the method comprises the steps of:

throwing away an extra bit when processing underflow operation (In Cota-Robles, this condition is defined as "overflow". However, Cota-Robles further discloses skipping a sample under this condition (column 10, lines 8-20), which matches the definition of applicant's underflow operation);

inserting a lost bit when processing the overflow condition (In Cota-Robles, this condition is defined as "underflow". However, Cota-Robles further discloses inserting a sample under this condition (column 9, lines 45-57), which matches the definition of applicant's overflow operation).

Cota-Robles fails to disclose the use of oversampling, each of the data is sampled by a plurality of sampling phases, determining an underflow circulation center point and an overflow circulation center point; processing an underflow operation and an overflow operation according to the underflow circulation center and the overflow circulation center.

Beladi teaches an oversampling correlator with a virtual clock phase for use in a telecommunication device (column 1, lines 6-9). Beladi also teaches the oversampling correlator using six sampling phases for one bit period (column 6, lines 5-7, FIG. 3) and selecting the optimum sampling phase, which provides the most accurate recovered data (column 7, lines 23-26). In Beladi, the six times oversampling correlator with shift provides for improved performance and reduces the circuitry (column 8, line 67, column 9, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the plurality of sampling phases and the determination of the optimum sampling phase, as suggested by Beladi with the operating method disclosed by Cota-Robles in order to implement oversampling, wherein each data is sampled by a plurality of sampling phases, determining an underflow circulation center point and an overflow circulation center point, and processing an underflow operation and an overflow operation according to the underflow circulation center and the overflow circulation center.

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Cota-Robles and Beladi fail to disclose the sampling phase that is a first sampling for each of the data is referred to as a leading edge sampling phase, the leading edge sampling phase with most occurrence times in a first one of at least one synchronous period being used as an initial leading edge phase.

Ichikawa teaches a bit synchronization circuit which performs oversampling of received data to determine content of the data (column 1, lines 111-13). Ichikawa also teaches the received data being sampled with plurality of samples and the result of the sampling synchronized with the first phase clock for output (column 7, lines 45-50). Ichikawa further teaches a state machine having 8 states --corresponding to current bit state and sample position within the bit (column 8, lines 1-6). The sample positions are cycled from 1-4 and back to 1 (FIG. 5). In Ichikawa, the synchronization circuit does not require high-speed clock to establish synchronization and is configured of digital circuitry, appropriate for mass production (column 9, lines 5-12). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use sampling cycle and state machine, as suggested by Ichikawa with the method disclosed by Cota-Robles and Beladi in order to implement the sampling phase that is a first sampling for each of the data is referred to as a leading edge sampling phase, the leading edge sampling phase with most occurrence times in a first one of at least one synchronous period being used as an initial leading edge phase.

Re claim 7, Cota-Robles Further discloses an operating method, for detecting and solving underflow (column 1, lines 9-14, column 3, lines 29-31), the method for a transmitter and a receiver to transmit and receive data by using different clock frequencies (column 1, lines 24-26), the receiver receives a plurality of received

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packages, each of the received packages includes a plurality of data (column 1, lines 19-23), the method comprises the steps of:

throwing away an extra bit when processing underflow operation (In Cota-Robles, this condition is defined as "overflow". However, Cota-Robles further discloses skipping a sample under this condition (column 10, lines 8-20), which matches the definition of applicant's underflow operation);

Re claim 7, Beladi further teaches the use of oversampling, each of the data is sampled by a plurality of sampling phases (column 6, lines 5-7, FIG. 3), determining an underflow circulation center point and processing an underflow operation according to the underflow circulation point (column 7, lines 23-26).

Re claim 7, Ichikawa further teaches the sampling phase that is a first sampling for each of the data is referred to as a leading edge sampling phase, the leading edge sampling phase with most occurrence times is used as an initial leading edge phase (FIG. 5).

Re claim 13, Cota-Robles Further discloses an operating method, for detecting and solving overflow (column 1, lines 9-14, column 3, lines 29-31), the method for a transmitter and a receiver to transmit and receive data by using different clock frequencies (column 1, lines 24-26), the receiver receives a plurality of received packages, each of the received packages includes a plurality of data (column 1, lines 19-23), the method comprises the steps of:

inserting a lost bit when processing the overflow condition (In Cota-Robles, this condition is defined as "underflow". However, Cota-Robles further discloses inserting a

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sample under this condition (column 9, lines 45-57), which matches the definition of applicant's overflow operation).

Re claim 13, Beladi further teaches the use of oversampling, each of the data is sampled by a plurality of sampling phases (column 6, lines 5-7, FIG. 3), determining an overflow circulation center point and processing an overflow operation according to the underflow circulation point (column 7, lines 23-26).

Re claim 13, Ichikawa further teaches the sampling phase that is a first sampling for each of the data is referred to as a leading edge sampling phase, the leading edge sampling phase with most occurrence times is used as an initial leading edge phase (FIG. 5).

Re claims 2, 8, and 14, Ichikawa further teaches the operating method, wherein each of the data is sampled (column 8, lines 1-8), the data is sampled by using one of the sampling phases after the leading edge sampling phase that is corresponding to each of the data (FIG. 4).

Allowable Subject Matter

Claims 3, 4, 9, 10, 15, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5, 6, 11, 12, 17, and 18 are allowed.

The following is an examiner's statement of reasons for allowance:

Re claims 3, 9, 15, the prior art fails to disclose or suggest the method as per claims 1, 7, and 13, wherein "the phase shift of the leading edge sampling phase that is located in between the $(n+1)/2$ th sampling phase and the $[(n+1)/2]+1$ th sampling phase

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is used as the underflow circulation center point and the overflow center circulation point”.

Re claims 4, 10, and 16 the prior art fails to disclose or suggest the method as per claims 1, 7, and 13, “the phase shift of the leading edge sampling phase that is located in the $[(m/2)+1]$ th sampling phase is used as the underflow circulation center point and the overflow center circulation point”.

Re claims 5, 11, and 17 the prior art fails to disclose or suggest “the phase shift of the leading edge sampling phase that is located in between the $(n+1)/2$ th sampling phase and the $[(n+1)/2]+1$ th sampling phase is used as the underflow circulation center point and the overflow center circulation point” and “the phase shift of the leading edge sampling phase that is located in the $[(m/2)+1]$ th sampling phase is used as the underflow circulation center point and the overflow center circulation point”.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoykov whose telephone number is (571) 272-4236. The examiner can normally be reached between 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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